UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/858,358	05/16/2001	Jonathan S. Yedidia		1770

7590 02/24/2004

Patent Department
Mitsubishi Electric Research Laboratories, Inc.
201 Broadway
Cambridge, MA 02139

EXAMINER	
ENG, MARSHALL S	

ART UNIT	PAPER NUMBER
2133	5

DATE MAILED: 02/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/858,358	YEDIDIA ET AL.	
	Examiner	Art Unit	
	Marshall S Eng	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5 and 6* is/are rejected.

7)☒ Claim(s) *3,4 and 7-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1.1 Applicant's arguments, filed 12 December 2003, with respect to the rejection(s)of claim(s) 1-7, 12, 15, 17 under 35 USC 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made below.

1.2 Objections to the drawings and specifications not stated below have been met and therefore withdrawn.

Specification

2.1 The disclosure is objected to because of the following informalities: the use of the mathematical term "loop" is consistently used, for example on lines 20-26 of page 17, while it appears that the mathematical term "cycle" should have been used in its place. The two terms, loop and cycle have markedly different definitions: a loop being an edge that connects a vertex to itself (clearly breaking a rule of bipartite graphs that no two vertices in the same set can be adjacent) while a cycle is set of edges that form a path (i.e. path being defined as an edge set with the same first node as last).

Appropriate correction is required.

Claim Objections

3.1 Claim 1 is objected to because of the following informalities: the word "size" in the 2nd line of the claim should not be deleted as it currently is. It appears that Applicant meant to delete only the ";" and not the word "size" as well.

3.2 Claims 5 and 6 are objected to because of the following informalities: the word "loop" is used while it is appears that the term that should be used is cycle.

3.3 Claim 9 is objected to because of the following informalities: a ":" should follow the word "comprising" at the end of the first line of the claim.

3.4 Claim 11 is objected to because of the following informalities: the spacing between the 2nd and 3rd lines needs to be adjusted so that they are either combined in one line or properly tabbed/indented as two limitations.

3.5 Claim 15 is objected to because of the following informalities: the word "and" should follow the ";" at the end of the 3rd line of the claim.

3.6 Claim 16 is objected to because of the following informalities: the word "and" should follow the ";" at the end of the 2nd line of the claim.

3.7 Claim 18 is objected to because of the following informalities: the ";" at the end of the 8th line of the claim (5th line of the 15th page of the filed Amendment) should be a ":"

3.8 Claim 18 is further objected to because of the following informalities: the ";" at the end of the 20th line of the claim (17th line of the 15th page of the filed Amendment) should be a ":"

3.9 Claim 18 is further objected to because of the following informalities: the ";" at the end of the 28th line of the claim (25th line of the 15th page of the filed Amendment) should be a ":"

3.10 Claim 18 is further objected to because of the following informalities: the phrase "transforming the numbers q sub aj" should be indented properly.

3.11 Claim 18 is further objected to because of the following informalities: there should be a "." at the end of the claim.

3.12 Claim 18 is further objected to because of the following informalities: the word erasure on line 2 of page 16 should apparently be "erasures."

Appropriate corrections are required.

Claim Rejections - 35 USC § 112

4.1 The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4.2 Claims 5 and 6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Where applicant acts as his or her own lexicographer to specifically define a term of a claim contrary to its ordinary meaning, the written description must clearly redefine the claim term and set forth the uncommon definition so as to put one reasonably skilled in the art on notice that the applicant intended to so redefine that claim term. *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999). The term "loop" in claims 5 and 6 is used by the claim to mean "cycle", while the accepted meaning is "an edge of a graph that connects a vertex to itself," see the "Graph Loop" definition from www.mathworld.com in the PTO-892 Notice of Reference Cited page. The term is indefinite because the specification does not clearly redefine the term.

Claim Rejections - 35 USC § 103

5.1 The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5.2 This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5.3 Claim(s) 1-3, 15-17 is/are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art 'Specifications' (hereinafter Specs) in view of Schikore et al. "Decimation of 2D Scalar Data with Error Control" (hereinafter Schikore).

As per claim 1,

Specs substantially teaches of evaluating an ecc code, see lines 20-25 of page 7. Specifically, on lines 23-25, Specs disclose the ability to determine (i.e. evaluate) the probability of a failure to decode which the examiner is interpreting as being equivalent to evaluating the failure rate (i.e. probability of failure to decode). Specs further teaches of defining a error-correcting code in terms of a parity check matrix, lines 15-20 of page

3, and of representing the parity check matrix as a bipartite (specifically a Tanner graph), see lines 4-10 of page 4.

Specs does not teach of iteratively renormalizing until a threshold. Nonetheless, Specs does teach of iterating the evaluation methods, see lines 20-25 of page 7.

Schikore, in an analogous art, teaches of decimation by deleting vertices and then minimizing the error introduced into the graph, see column 1 page 1, lines 9-17.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Specs to include the decimation techniques of Schikore. This modification would have been obvious because one of ordinary skill in the art would have been motivated by the suggestion provided by Schikore that the goal of decimation is to reduce the number of elements required to represent the sample data while not exceeding an error bound at any of the vertices, see column 1 page 2, section 3. Schikore further teaches that once decimated, the mesh (i.e. graph) will consist of a subset of the original points and data values and a new edge sets. Essentially, the decimation process is equivalent to renormalization due to the fact that both remove elements/vertices and then adjust the remaining values while trying to maintain a certain level of correctness

Further, it would have been obvious to one of ordinary skill in the art at the time the invention was made to iterate until a threshold. One of ordinary skill in the art would obviously want to continue deleting nodes/vertices until a certain point, i.e. certain number of nodes/vertices left or until a certain error level is reached. One would want to

do this so as to be able to stop the process before it removes all nodes/vertices or it removes one too many nodes/vertices and causing the too larger of an error.

As per claim 2,

It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the predetermined threshold a number of remaining nodes. As stated above in claim 1, if allowed to iterate repeatedly, the decimation/renormalization method would eliminate/delete *all* nodes unless it was told otherwise. Clearly, if the method were allowed to delete all nodes/vertices, there would be no graphical representation left and therefore nothing to evaluate. By setting a threshold to a number of nodes/vertices remaining, one of ordinary skill would ensure that at least X nodes/vertices remain after the decimation method so as to allow the evaluation to occur.

As per claim 3,

Specs further teaches of having variable nodes and checks nodes in a bipartite graph, see lines 4-23 of page 4.

Schikore further teaches of selecting a node/vertex (and of examining surrounding/connected nodes/vertices) and of deleting and adjusting (recalculating) the surrounding information, see bottom of column 1 page 2 section 3.1.

As per claim 15,

It would have been further obvious to one of ordinary skill in the art to select a set of criteria to evaluate error-correcting codes (i.e. failure rate and/or probability of failure to decode), generating a plurality of ecc codes, and searching the codes for an optimal

solution according to the criteria. One of ordinary skill in the art would be motivated to do so because, as Specs discloses first on lines 10-12 of page 1, those skilled in data communication and storage are always trying to find/generate optimal or near optimal ecc. Further, Specs discloses in lines 19-25 of page 2 of ways to generate near optimal codes and that decoding failures are one of a possible set of criteria used to determine optimal-ness. Therefore it would have been obvious to set the criteria for optimal ecc code searching (as Specs appears to have chosen decoding failure), generate ecc codes (as Specs has stated in line 19 of page 2) and then to search through the generated ecc codes to see which one is closest to being optimal. Obviously, if one of ordinary skill in the art were to set criteria and have a plurality of codes to look at, the artisan would know that one closest to the above mentioned criteria would be optimal and therefore should/would be chosen.

As per claim 16,

Specs further teaches of calculating probability of failure to decode at a node (being read as equivalent to an error rate), see lines 24-25 of page 7. Further, generating an optimal code would have been obvious once an evaluated error rate has been determined. Essentially, one of ordinary skill would look at the evaluated error rate at node and would be able to decide if the current error rate is optimal/near optimal. If it were, the artisan would easily be able to generate the corresponding ecc for the graph.

As per claim 17,

It would have been further obvious to one of ordinary skill in the art at the time the invention was made to evaluate an error rate (i.e. decoder failure or probability of failure to decode) on the normalized graph. One of ordinary skill in the art would have been motivated to do so by Schikore, who teaches that the idea of decimation is to reduce the number of elements required to represent the sampled data, see column 1 page 2 section 3. Further, since as in claims 15 and 16 renormalization is used to evaluate generated ecc to find an optimal one, it would have been obvious step to evaluate the renormalized/decimated/smaller representational graph. The purpose of the method is to evaluate codes, but also to an extent it is to find the optimal ones (as seen in claim 15). Since there already is the idea of wanting to find an optimal solution, it is obvious that an artisan would have to evaluate the renormalized representation in order to see if it optimal/near-optimal.

5.4 Claim(s) 5 and 6 is/are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art 'Specifications' (hereinafter Specs) and Schikore et al. "Decimation of 2D Scalar Data with Error Control" (hereinafter Schikore) as applied to claim 1 above, and further in view of Etzion et al. "Which codes have cycle-free tanner graphs" (hereinafter Etzion).

As per claim 5 and 6,

None of the above cited references of claim 1, Specs or Schikore, however, teach of bipartite graphs with/without loops (cycles).

Etzion, in an analogous art, teaches of bipartite (Tanner) graphs having and not having cycles, see title as well as all of column 2 on page 2174.

It would have been obvious to one of ordinary skill in the art at the time the invention was made that bipartite (especially Tanner) graphs are capable of having and not having cycles. One of ordinary skill in the art would be motivated to have or not have cycles in the bipartite (i.e. Tanner) graphs because cycles are well known properties of graphs. Etzion teaches of the cycle and cycle free Tanner (specialized bipartite) graphs in the preliminaries section, essentially teaching what is already known in the art about Tanner (bipartite) graphs.

Allowable Subject Matter

6.1 Claim 18 would be allowed if the objections noted above in paragraphs 3.7 – 3.12 were overcome.

The following is a statement of reasons for the indication of allowable subject matter: the claimed invention calls for a method for evaluating an error correcting code for a data block of finite size comprising: defining an ecc by a parity check matrix, representing the parity check matrix as a bipartite graph wherein the graph includes variable and check nodes that represent data and parity bits; iteratively renormalizing a node until a predetermined threshold is reached wherein the renormalization compress selecting a target node and a node to be renormalized; measuring a distance between the target node and every other node in the graph; if there exists a leaf variable node, renormalizing the one farthest from the target node, else if there exists a leaf check node, renormalizing the one farthest from the target node, else renormalize a non-leaf variable node located farthest from the target and having fewest directly connected check nodes; wherein the transmission channel is a binary erasure channel; decorating

the bipartite graph with probabilities of messages from variable to check and check to variable; renormalization of non-leaf variable nodes further comprising enumerating all check nodes connected to the non-leaf node, enumerating all other variable nodes connected to check nodes; wherein enumerating further comprises: enumerating all check nodes and variable nodes out to a predetermined distance from the target, constructing a logical argument to determine combinations of erasures causing a message to be an erasure; translating the logical argument into a transformation; and transforming the numbers q sub aj.

The prior art of record taken singly or in combination fails to teach or fairly suggest the claimed invention. Therefore, the examiner favors the allowance of claim 18, once the objections made in paragraphs 3.7-3.12 above are overcome.

6.2 Claims 4, 7-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7.1 The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Mathworld definitions of Graph Loop, Graph Cycle, Bipartite Graph.

b. Zarge et al. U.S. Patent No. 5,590,248

c. Nijman et al. "Efficient learning in Sparsely connected Boltzmann Machines"

d.Steedly et al. "A modified TLS-Prony method using data decimation"

7.2 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marshall S Eng whose telephone number is (703) 305-4638. The examiner can normally be reached on M-Th, 9 am to 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ME

mse

Guy J. Lamarre
for

Albert DeCady
Primary Examiner